FLIP-CHIP TECHNOLOGY – A STEP BEYOND IN SEMICONDUCTOR INDUSTRY

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Abstract. *Flip chip microelectronic assembly is the direct electrical connection of face-down electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology, which flip chip is replacing uses face-up chips with a wire connection to each pad. The main advantages obtained by introducing this advanced technology consists in size reduction, high performance, high operating frequencies and data rates, flexibility, reliability and low cost over other packaging methods. Few considerations from production, assembling and surface mounted technology are presented in the final part of this paper.*
Keywords: *flip chip, bonding, technology, packaging, SMT, SMD,.*

1. Introduction

There are several different types to place today one IC (Integrated Circuit) on PCB in the semiconductor industry. Starting with the oldest insertion method using IC in DIP package, passing through bonding technology that is using IC in die form, the manufacturers are using now the DCA (Direct Chip Attach). As a part of DCA, the flip chip and wafer-level CSP (Chip Scale Packaging) are the inevitable solutions for size, weight, and performance limitations.

Flip chip was not discovered nowadays. Basically this is a 25 year-old technology. The increasing of I/Os number for specific ICs is a fact and a new problem is arising: there is not enough space around the periphery of the device. To solve this, semiconductor manufacturers are moving to full area array or partial area array I/O designs that require a flip chip wafer bumping process. For this package, the I/O is entire surface distributed, not only on the periphery of the IC.

Area array layouts enhance signal propagation, power and ground distribution. Solder bump interconnections provide the lowest inductance, resistance and capacitance, which reduces high frequency delays and results in optimum signal speed and integrity. The flip chip technology delivers all of above advantages in less space than any other approach [1].

2. Bonding technology

The bonding technology is using the IC unpacked, in the die form, provided by the semiconductor maker before wire connection. The cost of the die is definitively saved because the maker is passing over the low yield plastic or metal packaging operations.

On the other hand, the manufacturer needs special machines and specialized technicians to attach, connect and protect the die on the substrate (PCB).

In the bonding technology, the IC in die form is first attached on the PCB using special glue, than is bonded using Aluminum, Gold or Copper wires (depending of the application), coated with epoxy material and tested in the final step.

Wire bonding is best characterized as a single-point-unit operation. Each bond is individually produced. Die on their substrate is moved through a wire bonder machine – a specialized machine that is using ultrasounds to connect the wire between the die's pad and the substrate lead. The machine's pattern recognition system identifies the die, transforms and corrects the taught locations for each bond, both on die and the PCB and individually moves to each location to produce an interconnection. In figure 1 are presented two interconnections between PCB and IC. In figure 2 we can see the entire IC bonded.

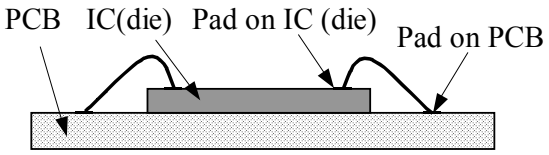

Figure 1. Die-PCB interconnections

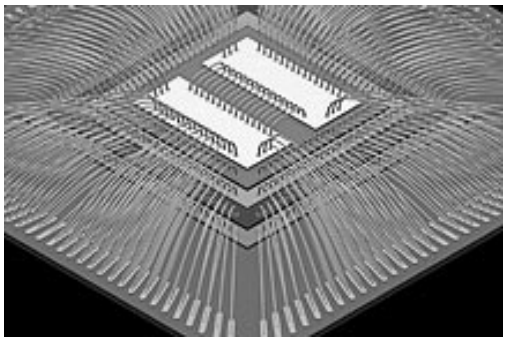

Figure 2. The IC bonded

To bond the entire IC we need n steps, where n is the number of interconnections between the IC in die form and the substrate (PCB). This why we call bonding a single-point operation process based [2].

3. Flip chip technology

The flip-chip technique reflects the significant progress made in the field of electronic packaging. The main characteristic of this kind of package is that the pads for connection are distributed on the entire surface of the die and the connection are made under the die and not in lateral like in bonding or classic package (DIP). With the flip-chip technique, the chip is mounted on the printed circuit board in such a way that the active side - or in other words the side that includes the structures - is turned towards the substrate (PCB). In figure 3 is presented one IC, in die form, produced with flip chip technique. It's easy to see in this picture the solder bumps for connections already attached on the die.

In order to obtain a final products using flip chip technology, we have to pass through two distinct levels [1]:

- Level 1: bumps attach;
- Level 2: attachment of the die with bumps on the substrate (PCB).

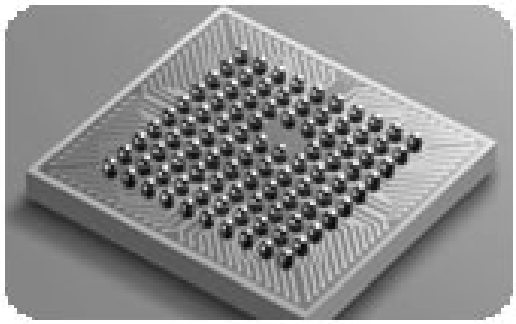

Figure 3. IC in flip chip technology

The flip chip process flow is depicted in figure 4.

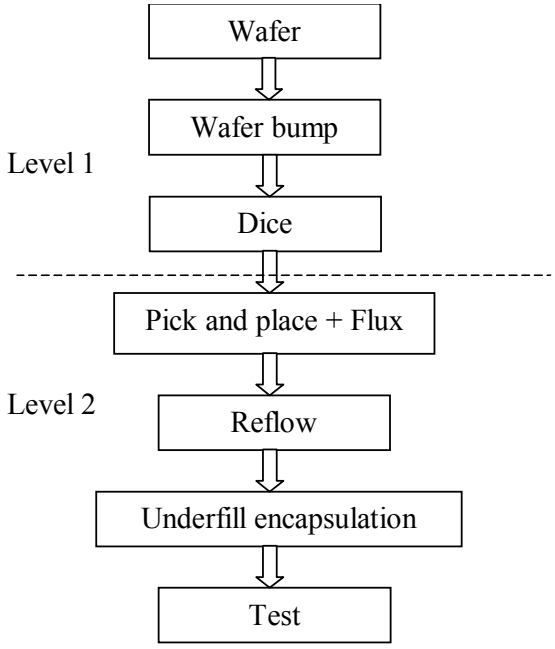

Figure 4. The flip chip process flow

The interconnection process is completed by means of so-called bumps that were mounted on the chip in the first level of the process [3].

The flip chip technology is a wafer-scale operation based. Bumps (solder balls) are formed on an entire wafer so, for up to thousands dies in one step. The maximum numbers of bumps attached on a die is around

6000 nowadays. In the assembling process, each bump will make a connection between the IC (in die form) and the substrate. No wire is necessary for this connection. Only after all bumps are placed, the wafer is diced - spitted in individual IC - resulting IC in die form with bumps, named flip chip.

During the assembly process, the individual die are picked, fluxed and placed on the PCB or any substrate. Special equipments vacuum based are used for these operations. The flux used to keep the IC (flip chip) on substrate must be sticky enough to hold the die in place for handling through reflow. The pick and place equipment must also align the flip chip on substrate. In the next operation, in reflow, all solder bumps are reflowed above their melting point to form the interconnection between die's pads and substrate (PCB).

In some flip chip technologies are necessary supplementary operations like underfilling (a specialized encapsulant that fills the gap between chip and substrate to protect the delicate interconnect structure against thermo-mechanical behavior of the chip) and encapsulation (a method to protect the IC in die form) [4]. In the final step, the IC attached is tested in order to check if all connections are well done.

During whole process we are handling the wafers, the die or the substrates with die attached. In the flip chip technology we are never working with one connection only, than all connections between die and substrate are made in one step. It is never a single-point operation like in bonding technology. This is one of the major advantages of the flip chip technology that produce a real increase in the production throughput. In addition, the contact via bumps reduces the amount of space required not just in terms of area (which is up to 95%), but also in the height of the structure, which can be up to 40% lower than in wire-bonding technique. These are the main advantages of this new technology.

Solder bumping

The key part of the flip chip technology is the solder bumping process. In the flip chip technology, the solder (in the bump form) is applied over the die's pads on all 5-8' wafer, before to be broken in individual chips. This why it's usually to meet the term "wafer bumping".

Generally, wafer bumping is defined as the process by which the solder, in the form of bumps or balls, is applied to the device at the wafer level. The use of wafer bumping is driven either by performance, form factor or array interconnect requirements. The ability to properly design the device for bumping will have direct bearing on manufacturability, reliability, and cost savings from wafer fabrication through component assembly [5].

The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

The solder bumping process first requires that an under bump metallization (UBM) be placed on the chip bond pads, by sputtering, plating, or other means, to replace the insulating aluminium oxide layer and to define and limit the solder-wetted area. Solder is then deposited over the UBM by evaporation, electroplating, screen-printing solder paste, or needle-depositing. The solder bumping process is depicted in figure 5.

The UBM (Under Bump Metallurgy) serves as a platform for the solder bump as well as a metallurgic system that is specifically designed to connect the wafer metallurgy to the solder bump metallurgy. The goal of this solder bumping process is to produce a highly reliable and stable structure. The UBM overlaps the wafer passivation layer to protect the wafer circuitry from corrosion, to get a low ohmic

contact to the final metal pad, to create a diffusion barrier against the reaction between solder and Al, a.s.o..
Dielectric layers are used to repassivate wafers and to redistribute the I/O pattern (from the periphery to the entire die surface). Repassivation also planarizes the device, provides a stress buffer layer, and protects IC metal from the UBM etch process.

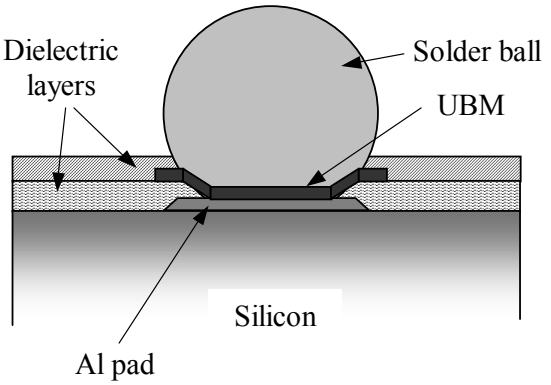

Figure 5. The solder bumping process

The flip chip technology is recently introduced and it competes with the bonding technology in the assembling processes field. The EMS (Electronics Manufacturing Services) companies can easily introduce this new technology but they usually have to use a transformed IC. Only few IC can be now provided by wafer makers in DCA package. The flip-chip wafers were originally designed with peripheral pad layouts for wire bonding (pads distributed on periphery). This die have to be transformed in a die with pads distributed over the surface The most important step in this transformation is the redistribution of the peripheral bond pads to an area array design. Dielectric and metal layers are added to redistribute and connect the aluminum bond pads to area array bumps [5]. The die structure with redistributed pads is presented in figure 6.
There are already few providers for bumping service and for this transformation (redistribution): Kulicke and Soffa, Fijutsu, Amkor, Apack, Shinko. They are offering this technology that can be easily accommodated

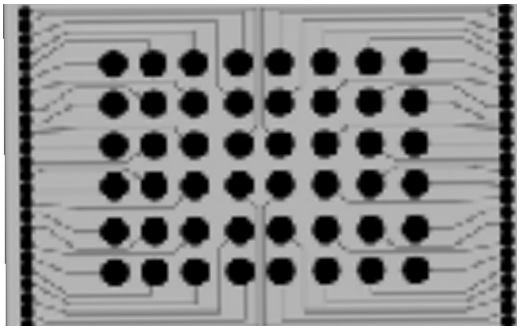

Figure 6. Redistribution of the peripheral bond pads

with a wide variety of wafer materials and configurations. This include the prototype realization, many passivation and wafer types, up to 6,000 bumps per die, pad's redistribution, etc. Usually they are working with 4-8 inch wafer but 12 inch wafer can also be used in special configurations. The pitch is depending of specific flip chip technology and could be between 0,1 mm (standard flip chip) and 1mm (Ultra CSP).

4. Few consideration about the assembly process for flip chips.

In production, beside the flip chip die, we need a substrate (PCB) designed for flip chip attachment. The migration from wire-bonded package to flip chip package has a significant impact on the design of substrate. The laminate substrate becomes much more complex and costly. In many cases, the substrate cost exceeds the silicon cost [7].
The IC attachment is realised during the assembly process. Assembly operations include handling, placing, fluxing, and solder joining. The bumped die packaging, the solder bump, the substrate (or board material), the assembly equipment, the final product characteristics and the cost influence the assembly process. For manufacturing, the machine selection is the single most critical factor in establishing the balance between throughput and flexibility in flip chip assembly process.
Bumped die may be transported in waffle packs on tape or in reels. Tape and reel requires a special design for carrying flip chips. Placing the

bumped die may be by fine-pitch surface-mount equipment or by high-accuracy flip chip placement equipment. In both cases, the die must be aligned with the bond pads on the substrate (PCB) before placement.

The preferred fluxes used to connect the die to the substrate are no-clean fluxes. The soldering process could use a conventional belt reflow or a hydrogen reflow.

One function of the solder bump is to provide a space between the chip and the board. In the last stage of assembly process, this under-chip space is usually filled with a non-conductive underfill adhesive, joining the entire surface of the chip to the substrate. The underfill protects the bumps against accidental moisture and provides additional mechanical strength to the assembly. However, its most important purpose, particularly with solder bumps connections on large die or to organic substrates, is to compensate for thermal expansion differences between the chip and the substrate. The underfill material keeps together the chip and the substrate so that differences in thermal expansion do not break or damage the electrical connection of the bumps. Also, the underfill material has been found to increase the fatigue life of solder bumps. The underfill material must also be compatible with the flux and this constrain is solved for many usual non-clean and clean modern fluxes.

Sometimes, in production, a cleaning step to remove the flux residues may be required before underfilling. This is not a compulsory step in the assembly process but usually the production management will introduce it in order to reduce the amount of rework and to increase the production yield and the reliability of the final product. Depending of the product and equipments used in flip chip assembly process, this step is often the best solution to avoid underfill quality problems.

Underfill may be needle-dispensed along one or two edges of each chip. It is drawn into the under-chip space by capillary action, and heat-cured to form a permanent bond. The durst or flux residues could create underfill holes under the flip chip. Even a clear surface could issue a non-equal distribution of the underfill material. Flow characteristics, adhesion to both chip and board and cure time are key concerns to correct this problem. We need also to carefully set-up the reflow, to choose a specific cure profile depending of the flip chip, underfill material and flux characteristics. Before starting the mass production for a specific product, a set-up lot have to be produced for finding the appropriate parameters for all equipments involved. We have then to keep under a permanent control all these parameters during mass production.

One important station in the assembly flip chip process is the rework station. The main role of this station is to avoid scrapping the entire boards with high cost devices attached on them because testing has determined that a flip chip is defective. The flip chip rework is possible only if a reworkable underfill material is used in assembly process [8]. This kind of underfill material is now available from such companies as Loctite, Emerson & Cuming and IBM. The goal of the rework station is to physically remove the defective flip and replace it with a good die.

The rework process begins with heating the substrate to a temperature below the melting point of solder. The chip is then spot heated to melt the solder connections and break down the underfill. In this moment the chip is gripped mechanically and then twisted or sheared away from the circuit. Any residual solder and underfill are cleaned off the substrate. Once cleanup of the substrate is complete, a new chip can be aligned, bonded, reflowed, and underfilled.

To successfully remove the defective flip chip from the substrate, the process must be compatible with the assembled board and the components attached to it. It requires a machine that is equipped for bottom-side heating of the substrate to temperatures up to 200°C, with the most common temperature range being 125° to 150°C.

The rework station should also have a hold-down device for the substrate during removal of

the chip. In those cases where the substrate is fragile or exceptionally thin (PC cards or FR4 under 1mm), a custom fixture may be required.
The rework station could improve the production yield with 2-4 % for low complexity boards and 5-10% for complex boards. This is the reason for EMS companies to invest in good equipments for rework flip chip components.

5. Flip chip versus bonding-wire from production point of view.

Current flip-chip designs are in production with maximum 6000 bumps per chip at 200 µm pitch and about 1000 bumps for 125 µm pitch. Current mass production for wire bonding is in the 50 µm range, but a production capability of 35-µm is already possible in the technologic advanced EMS because the bonding equipments are already on the market. All flip chip devices use solder interconnects. The solder melts and provides a mechanically strong joint with low electrical resistance. The best solder alloys for flip-chip applications are the Sn/Ag/Cu with the possible inclusion of an additional element. Other new alloys used are 35Pb/65Sn or 95Pb/5Sn. Typical electrical solders contain lead are expected to be replaced by lead-free alloys (much more ecologic).
The bonding technology is working with a finer pitch (up to 35 µm). The main advantage of bonding is that there is a true weld, joining the two metals through an inter-metallic phase. Fine-pitch wire bonding is also a complicated process. Molding fine-pitch wire bonds requires additional process capabilities to avoid wire sweep and deflection. Finer diameter wires required to achieve fine pitch are not as strong or as stiff as larger diameter wires. To address these constraints, manufacturers are developing higher strength wire alloys, copper-wire for bonding and encapsulant formulations to minimize sweep at fine pitches and with long wires. Cost comparisons and analyses are highly dependent on I/O number and substrate. Optimum substrate choices often change through the life of a product but depending on production volume.
Electrical performance or form factor are usually the most important criteria for a change from wire bonding to flip chip process in mass production. The communication market, requesting product for 1,8 GHz, 2,4 GHz and over is the main customer. Regarding the form factor, wafers designed specifically for area array flip-chip may have smaller die, because peripheral bond-pad layout requires a larger die perimeter to design the required I/O. Die size is a dominant factor in the cost of a chip and represents a significant advantage for flip-chip in communication industry where very small components and wires are requested due to electromagnetic constrains.

Table 1

Parameter	Flip chip technology	Wire-bonding technology
Minimum pitch	100 µm peripheral/ 140 µm array	35 µm peripheral only
Maximum connections number per die	6000	500
Required board area *)	5-10%	75-80%
Weight (compared with SMD)	5-10%	10-15%
Working frequency *)	50 …… 1000% (3GHz available)	Similar
Connection material	64Sn/1Ag/35Cu; 35Pb/65Sn; 95Pb/5Sn lead free alloys	Al, Au, Ag
Cost per connection over 5000 I/O (USD)	<0,010	0,01…..0,02
Cost per connection under 50 I/O (USD)	0,02…..0,05	0,01…..0,02
Replacing the IC in rework station *)	Similar	25…30%
Cost per die *)	40-50%	60-80%

* compared with traditional SMD plastic package

In table 1 we find for comparing few main characteristics for these two technologies.

6. Conclusions

Worldwide flip chip consumption was about 1 million units on 2003, with a projected annual growth rate of nearly 50% per year. Semiconductor manufacturers currently bump for flip chip assembly about 5% of wafers produced and are expected to be bumping over 10% within a few years.

The boom in flip chip packaging results both from flip chip's advantages in size, performance, flexibility, reliability, and cost over other packaging methods and from the widening availability of flip chip materials, equipment, and services.

Eliminating packages and bond wires reduces the required board area by up to 95%, and requires far less height and weight. Flip chip is the simplest minimal package used in electronic industry. Both wire bonding and flip-chip will continue to coexist but both technologies will split the market with traditional die packing that will still cover 70-80 % of the market in next decade. The flip-chip is advantageous as production method. As the flip-chip infrastructure is established, costs will be reduced and the application space will broaden.

Where applications can be produced by wire bonding, its cost advantages for low I/O number will determine the interconnect method. But the high frequency applications (over 1,8 GHz) will be the main market for flip chip technologies (or Direct Chips Attach - DCA - technologies, in general terms).

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